Study on differential mode conducted interference of trigger circuit of high-power thyristors in pulsed power supply

Jiu-fu Wei[1], Xiang-rong Liu[1], Hong-e Luo[1], Zhen-xiao Li[1], Bao-ming Li[1,2]
[1]National Key Laboratory of Transient Physics, Nanjing University of Science and Technology, Nanjing, China
[2]China Academy of Ordnance Science, Beijing, China

1. Introduction

High-power thyristor is widely adopted as a power switching device in PPS [1]-[3]. Compared with other similar switching devices, high-power thyristors have a relatively lower-cost in applications of high voltage and current. However, trigger pulses of high-power thyristors must be with high accuracy in PPS, which directly affects the performance of PPS.

The trigger pulse of high-power thyristors is one of the key factors affecting the reliability of a PPS. If the trigger pulse of high-power thyristors is abnormal, PPS will also be abnormal. The trigger pulse of high-power thyristors can affect its accuracy that is closely related to triggering consistency of high-power thyristors and the accuracy of the high-power output pulse of PPS.

Plenty of pulse transformers and SMFETs applied in trigger circuit of high-power thyristors can generate voltage change rate *du/dt* and current change rate *di/dt*, which can result in electromagnetic conducted interference (EMCI) problems [4]-[6]. Generally, the trigger pulse is sensitive to EMCI in trigger circuit of high-power thyristors.EMCI is usually divided into common-mode conducted interference (CMCI) and differential-mode conducted interference (DMCI).To improve the reliability of PPS, this paper aims to discuss DMCI in a trigger circuit of high-power thyristors and find some effective methods to suppress it. To verify the theoretical analysis, the peak (PK) spectrums of DMCI are measured in the frequency range of 10kHz-10MHz.

2. Principle of DMCI in trigger circuit of high-power thyristors

2.1. Principle of trigger circuit of high-power thyristors

The principle of a trigger circuit of high-power thyristors is shown in Figure 1. Figure 1(a) is the schematic diagram of a trigger circuit of high-power thyristors and Figure 1(b) is the circuit principle of a one-stage trigger circuit of high-power thyristors. The trigger circuit of high-power thyristors is mainly composed of powerful trigger units, MCU control units, and remote control computer units. The powerful trigger units are mainly composed of a DC power source module and powerful trigger pulse forming modules (PFMs). The DC power source module usually applies the principle of switching power supply (SPS) to convert the AC power source from an uninterruptible power supply (UPS) into a DC power source. A power trigger PFM mainly is composed of a SMFET and a pulse transformer. The trigger circuit of high-power thyristors can be divided into one-stage trigger circuit of high-power thyristors, two-stage trigger circuit of high-power thyristors,…, and *N*-stage trigger circuit of high-power thyristors according to the number of powerful trigger units.

Figure 1. Principle of a trigger circuit of high-power thyristors. **(a)** Schematic diagram of a trigger circuit of high-power thyristors. **(b)** Circuit principle of a one-stage trigger circuit of high-power thyristors.

2.2. High-frequency parasitic parameters of key components

2.2.1. High-frequency parasitic parameters of a pulse transformer

In a powerful trigger unit, the high-frequency parasitic parameter of a pulse transformer can worsen DMCI [7]-[10]. The distributed parasitic capacitance model of a pulse transformer is shown in Figure 2(a). The lumped parasitic parameter model of a pulse transformer is shown in Figure 2(b).

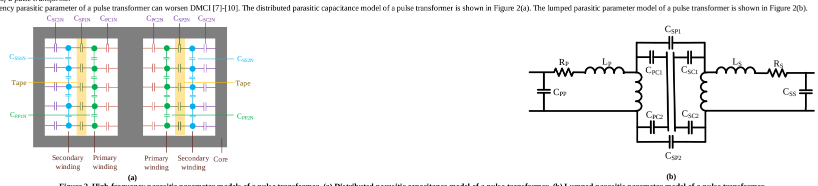

Figure 2. High-frequency parasitic parameter models of a pulse transformer. (a) Distributed parasitic capacitance model of a pulse transformer. (b) Lumped parasitic parameter model of a pulse transformer.

2.2.2. High-frequency parasitic parameters of SMFET

A SMFET has three pins: drain, source, and gate. There is a parasitic capacitance at the PN junction of every two pins. Figure 3 shows the equivalent parasitic parameter model of a SMFET. L_D is the high-frequency parasitic inductance at the drain, L_S is the high-frequency parasitic inductance at the source, R_G is the equivalent resistance of the gate, C_{DG} is the high-frequency parasitic capacitance between the drain and the gate, C_{GS} is the high-frequency parasitic capacitance between the gate and the source, and C_{DS} is the high-frequency parasitic capacitance between the drain and the source [13]-[14].

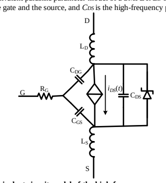

Figure 3. Equivalent circuit model of the high-frequency parasitics of a SMFET.

2.3. Principle of the DMCI in trigger circuits of high-power thyristors

To meet the requirements of volume limitation, several trigger circuit units usually share a DC power source forming a multi-stage trigger circuit of high-power thyristors, which can inevitably worsen DMCI. Based on the parasitic parameter models of the pulse transformer and SMFET, Figure 4 shows the principle of DMCI in the trigger circuit of high-power thyristors.

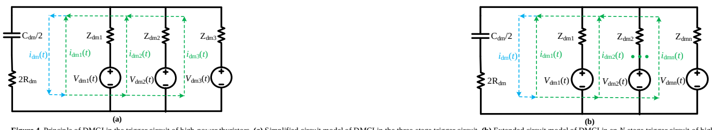

Figure 4. Principle of DMCI in the trigger circuit of high-power thyristors. **(a)** Simplified circuit model of DMCI in the three-stage trigger circuit. **(b)** Extended circuit model of DMCI in an *N*-stage trigger circuit of high-power thyristors.

2.4. Suppressive methods of DMCI in trigger circuit of high-power thyristors

Generally, implanting an EMI filter at the power input port of a trigger circuit of high-power thyristors can effectively suppress DMCI. The principle of a one-stage EMI filter is shown in Figure 5.

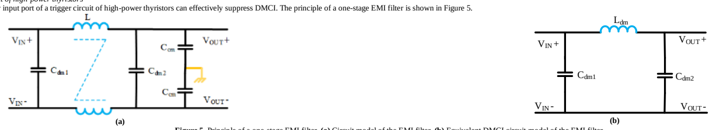

Figure 5. Principle of a one-stage EMI filter. **(a)** Circuit model of the EMI filter. **(b)** Equivalent DMCI circuit model of the EMI filter.

3. Experimental results

Figure 6 shows the measured PK spectrums of DMCI in a one-stage trigger circuit of high-power thyristors (f_t=50KHz, 100kHz, and 150kHz, respectively; load resistance R_{load}=1kΩ). Figure 6 illustrates that in the frequency range of 10kHz-10MHz, with the increase of trigger frequency, PK values of the DMCI spectrums also increase, indicating that the DMCI becomes heavier with the increase of trigger frequency.

Figure 7 shows the measured PK spectrums of DMCI in trigger circuits of high-power thyristors when several different EMI filtering components are added at the power input port (f_t=50KHz, R_{load}=1kΩ). Figure 7 displays that the leakage inductance of CM choke can be used to suppress DMCI if DMCI is relatively minor in a trigger circuit of high-power thyristors; DM capacitors and DM inductors can be implanted in an EMI filter if DMCI is relatively heavy in a trigger circuit of high-power thyristors.

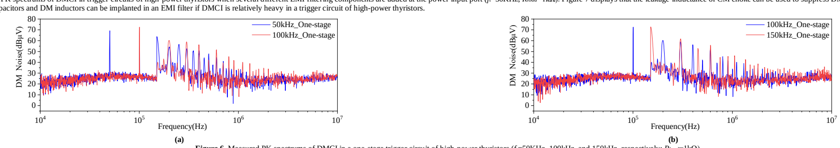

Figure 6. Measured PK spectrums of DMCI in a one-stage trigger circuit of high-power thyristors (f_t=50KHz, 100kHz, and 150kHz, respectively; R_{load}=1kΩ).

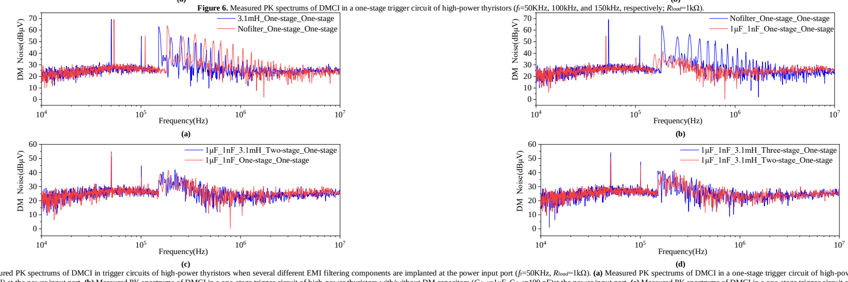

Figure 9. Measured PK spectrums of DMCI in trigger circuits of high-power thyristors when several different EMI filtering components are implanted at the power input port (f_t=50KHz, R_{load}=1kΩ). **(a)** Measured PK spectrums of DMCI in a one-stage trigger circuit of high-power thyristors with/without a CM choke (*L*=3.1mH) at the power input port. **(b)** Measured PK spectrums of DMCI in a one-stage trigger circuit of high-power thyristors with/without DM capacitors (C_{dm1}=1μF, C_{dm2}=100 nF)at the power input port. **(c)** Measured PK spectrums of DMCI in a one-stage trigger circuit of high-power thyristors with DM capacitors (C_{dm1}=1μF, C_{dm2}=100 nF) at the power input port and in a two-stage trigger circuit of high-power thyristors with a one-stage EMI filter (*L*=3.1mH, C_{dm1}=1μF, and C_{dm2}=100 nF) at the power input port. **(d)** Measured PK spectrums of DMCI in a two-stage/three-stage trigger circuit of high-power thyristors with a one-stage EMI filter (*L*=3.1mH, C_{dm1}=1μF, and C_{dm2}=100 nF) at the power input port.

4. Conclusion

To improve the reliability of PPS, the DMCI in the trigger circuit of high-power thyristors is investigated based on the following aspects: high-frequency parasitic parameters of key devices; the principle of DMCI in the trigger circuits of high-power thyristors; suppression methods of DMCI. According to the theoretical analysis and experimental results, EMI filtering components(DM capacitor/inductor, CM choke, EMI filter and so on) can effectively suppress DMCI. Besides, limiting high-frequency parasitic parameters of key devices is also an effective way to suppress DMCI.

References

[1] Dai L, Wang Y, Zhang Q, et al 2013 Effect of sequence discharge on components in a 600-kJ PPS used for electromagnetic launch system[J] *IEEE T Plasma. Sci* vol 4 pp 1300-1306
[2] Guo X, Dai L, Zhang Q, et al 2014 Influences of electric parameters of pulsed power supply on electromagnetic railgun system[J] *IEEE T Plasma. Sci* vol 43 pp 3260-3267
[3] Li W B, Xin W, Feng Q, et al 2013 Some Considerations of the Pulse Power Switch Centered on Thyristor Device[C] *Applied Mechanics and Materials* vol 336 pp 60-64
[4] Wang Z J, Wang S, Kong P G, et al 2011 DM EMI noise analysis for critical conduction mode PFC *IEEE 26th Annual APEC* pp 1475-1481
[5] Tarateeraseth V, Maneenopphon T and Khan-Ngern W 2007 The comparison of EMI and electrical performances of high frequency transformer windings for SMPS applications *IEEE Power Conversion Conference-Nagoya* pp 435-440
[6] He J P, Wei C and Jian G J 2005 Model and analysis on common-mode conducted EMI of a switched mode power supply *Proceedings of the CSEE* vol 25 pp 50-55
[7] Sha Z Y, Ge J Y and Wu R H 2003 Design Key Point of High Frequency Transformer of Single-chip Switching Power Supply Power Supply Technology And Applications vol.6 pp 266-268
[8] Huang K W, Li J, Fan N J, et al 2008 Analysis and Simulation of the Influence of Transformer Parasitics to Low Power High Voltage Output Flyback Converter IEEE International Symposium on Industrial Electronics pp 305-310
[9] Dong J Q, Chen W, Lu Z Y 2007 Modeling and analysis of capacitive effects in high-frequency transformer of SMPS[J] Proceedings Chinese Society of Electrical Engineering vol 27 pp 111-126
[10] Pang T Y, Ling Y S, et al 2017 Study on the Parameter Matrix of the Winding Field of a High Frequency Transformer for a Switching Power Supply Telecom Power Technology vol 34 pp7-10
[11] Liu C, Qi L, Cui X and Zhao G L 2017 An experimental method for extracting parasitic capacitances of high-voltage high-frequency transformers Journal of North China Electric Power University vol 44 pp 1-8
[12] Liu C, Qi L, Cui X and Zhao G L 2017 Impact mechanism and optimization of parasitic parameters on transfer characteristics of high-power high-frequency transformers Journal of North China Electric Power University vol 44 pp 7-14
[13] Cheng L, Chen Q and Li G L 2014 Mathematical Modeling and Loss Analysis of Power MOSFET Based on Parasitic Parameters Journal of East China University of Science and Technology (Natural Science Edition) vol 40 pp 740-745
[14] Chen Q, Wang Q J, Jiang W D and Hu C G 2008 Analysis of Switching Losses in Diode-Clamped Three-Level Converter Transactions of China Electrotechnical Society vol 23 pp 68-75
[15] Wang S, Lee F C, Odendaal W G 2005 Characterization and parasitic extraction of EMI filters using scattering parameters[J] IEEE Transactions on Power Electronics vol 20 pp 502-510.
[16] Wang S, Lee F C and Odendaal W G 2004 Controlling the parasitic parameters to improve EMI filter performance[C] Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition APEC vol 1 pp 503-509
[17] Wang Shuo, W. G. Odendaal and F. C. Lee 2004 Extraction of parasitic parameters of EMI filters using scattering parameters Conference Record of the 2004 IEEE Industry Applications Conference vol 4
[18] Yue, Lingling and Xiaodong Zhang 2009 The design of a multifunctional test apparatus-LISN Used for conduction interference testing 2009 3rd IEEE International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications